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M Rosenblum, SA Herrod, E Witchel, A Gupta - Parallel & Distributed Technology: Systems & Applications, ..., 1995 - ieeexplore.ieee.org
... Although the direct-**execution** mode is fast, it provides ... uses on-the-fly object code **translation** to dynamically ... time and a breakdown of **instructions** executed. ...
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PicoJava: A Direct **Execution** Engine For Java Bytecode - group of 5 »
H McGhan, MO'Connor - Computer, 1998 - portal.acm.org
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Embra: fast and flexible machine **simulation** - group of 7 »
E Witchel, M Rosenblum - Proceedings of the 1996 ACM SIGMETRICS international ..., 1996 - portal.acm.org
... addressspaces.In addition to MMU **translation**, features of ... stop the current flow of **execution**, and invoke ... Embra needs to support **instructions** for manipulating ...
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Using the SimOS Machine Simulator to Study Complex Computer Systems - group of 9 »
M ROSENBLUM, E BUGNION, S DEVINE, SA HERROD - ACM Transactions on Modeling and Computer **Simulation**, 1997 - portal.acm.org
... of the actual interleaving of the **instructions** executed ... Direct **execution** was frequently used to position the workloads ... in favor of the binary **translation** approach ...
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2. **Complete computer system simulation: the SimOS approach**
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4. **Uniprocessor virtual memory without TLBs**
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6. **Modular Minicomputers Using Microprocessors**
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7. **Developing the AMD-K5 architecture**

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1 Embra: fast and flexible machine simulation

Emmett Witchel, Mendel Rosenblum

May 1996 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1996 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '96**, Volume 24 Issue 1

Publisher: ACM Press

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This paper describes Embra, a simulator for the processors, caches, and memory systems of uniprocessors and cache-coherent multiprocessors. When running as part of the SimOS simulation environment, Embra models the processors of a MIPS R3000/R4000 machine faithfully enough to run a commercial operating system and arbitrary user applications. To achieve high simulation speed, Embra uses dynamic binary translation to generate code sequences which simulate the workload. It is the first machine simu ...

2 Performance of the VAX-11/780 translation buffer: simulation and measurement

Douglas W. Clark, Joel S. Emer

February 1985 **ACM Transactions on Computer Systems (TOCS)**, Volume 3 Issue 1

Publisher: ACM Press

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A virtual-address translation buffer (TB) is a hardware cache of recently used virtual-to-physical address mappings. The authors present the results of a set of measurements and simulations of translation buffer performance in the VAX-11/780. Two different hardware monitors were attached to VAX-11/780 computers, and translation buffer behavior was measured. Measurements were made under normal time-sharing use and while running reproducible synthetic time-sharing work loads. Reported measure ...

3 Efficient instruction cache simulation and execution profiling with a threaded-code interpreter

Peter S. Magnusson

December 1997 **Proceedings of the 29th conference on Winter simulation WSC '97**

Publisher: ACM Press, IEEE Computer Society

Full text available: pdf(912.22 KB) Additional Information: full citation, references, index terms

4 Trace-driven memory simulation: a survey

Richard A. Uhlig, Trevor N. Mudge

June 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 2